AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A non-volatile semiconductor storage apparatus comprising:

a memory cell array which has unit cells arranged in a rectangular matrix shape, said unit cell including:

a memory cell field effect transistor having a floating gate and a control gate; and

a select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said floating gate and control gate extending to a position above a gate of said select field effect transistor, top and bottom surfaces of said floating gate and said control gate in said position being parallel to top and bottom surfaces of said gate of said select field effect transistor, an insulating layer formed directly below said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer in a region to be an active region of said unit cell.

2. (Previously Presented) A non-volatile semiconductor storage apparatus having a memory cell array having unit cells, said unit cell including a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate and a control gate, and said select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said storage apparatus comprising:

a first semiconductor layer composing a portion of said floating gate and a gate of said select field effect transistor;

a second semiconductor layer formed on said first semiconductor layer in said memory cell field effect transistor, said second semiconductor layer not contacting said tunneling gate oxide layer, a lower surface of said second semiconductor layer being located at a height at least equal to a height of an upper surface of said first

semiconductor layer, said second semiconductor layer composing another portion of said floating gate and extending to a position above said gate of said select field effect transistor;

a first insulation layer which insulates said first semiconductor layer from said second semiconductor layer on said select field effect transistor, said first insulation layer contacting said first semiconductor layer;

a second insulation layer formed on said second semiconductor layer; and

a third semiconductor layer formed on said second insulation layer and composing said control gate

the third semiconductor layer, the second insulation layer, and the second semiconductor layer being etched using a single photoresist film as a mask,

an insulating layer formed directly below said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer.

3. (Cancelled)

4. (Cancelled)

5. (Previously Presented) The non-volatile semiconductor storage apparatus according to claim 1, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells.

6. (Previously Presented) The non-volatile semiconductor storage apparatus according to claim 2, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells.

7. (Currently Amended) [[A]] <u>The</u> non-volatile semiconductor storage apparatus <u>of claim 1,</u> ~~comprising:~~

~~a memory cell array which has unit cells arranged in a rectangular matrix shape, said unit cell including:~~

~~a memory cell field effect transistor having a floating gate and a control gate; and~~

~~a select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said floating gate and control gate extending to a position above a gate of said select field effect transistor, top and bottom surfaces of said floating gate and said control gate in said position being parallel to top and bottom surfaces of said gate of said select field effect transistor, an insulating layer formed directly below said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer, said non-volatile semiconductor storage apparatus~~ further comprising:

a source line commonly connecting sources of said select field effect transistors arranged in a first direction;

a semiconductor layer connecting said source and said source line for said each select field effect transistor; and

a drain diffusion layer shared between adjacent memory cell field effect transistors in a second direction in said unit cells.

8. (Previously Presented) [[A]] The non-volatile semiconductor storage apparatus of claim 2, ~~having a memory cell array having unit cells, said unit cell including a memory cell effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate and a control gate, and said select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said storage apparatus comprising:~~

~~a first semiconductor layer composing a portion of said floating gate and a gate of said select field effect transistor;~~

~~an insulating layer provided directly below said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer;~~

~~a second semiconductor layer formed on said first semiconductor layer in said memory cell field effect transistor, said second semiconductor layer not contacting said tunneling gate oxide layer, a lower surface of said second semiconductor layer being located at a height at least equal to a height of an upper surface of said first semiconductor layer, said second semiconductor layer composing another portion of said floating gate and extending to a position above said gate of said select field effect transistor;~~

~~a first insulation layer which insulates said first semiconductor layer from said second semiconductor layer on said select field effect transistor, said first insulation layer contacting said first semiconductor layer;~~

~~a second insulation layer formed on said second semiconductor layer; and~~

~~a third semiconductor layer formed on said second insulation layer and composing said control gate,~~

~~the third semiconductor layer, the second insulation layer and the second semiconductor layer being etched using a single photoresist film as a mask,~~

~~said non-volatile semiconductor storage apparatus~~ further comprising:

a source line commonly connecting sources of said select field effect transistors arranged in a first direction;

a semiconductor layer connecting said source and said source line for said each select field effect transistor; and

a drain diffusion layer shared between adjacent memory cell field effect transistors in a second direction in said unit cells.

9-18. (Cancelled)

19. (New) The non-volatile semiconductor storage apparatus of claim 1, wherein a common region forming the source of the memory cell field effect transistor and the drain of the select field effect transistor is defined by a tunnel insulating film of the

memory cell field effect transistor and a gate insulating film of the select field effect transistor.

20. (New) The non-volatile semiconductor storage apparatus of claim 2, wherein a common region forming the source of the memory cell field effect transistor and the drain of the select field effect transistor is defined by a tunnel insulating film of the memory cell field effect transistor and a gate insulating film of the select field effect transistor.

21. (New) A non-volatile memory comprising:

a semiconductor substrate;

a select transistor including a gate insulating film formed on a first region of said semiconductor substrate and a select gate formed on said gate insulating film;

a tunnel insulating film formed on a second region of said semiconductor substrate; and

a memory transistor including a floating gate formed on said tunnel insulating film and extending to a position above said select gate, a common diffusion layer formed on a third region of said semiconductor substrate defined by said first region and said second region and shared with said select transistor and a control gate facing said floating gate.